Claims

We Claim:

1. A. computer-implemented method for generating a hardware implementation of graphical code, the method comprising:

creating a graphical program, wherein the graphical program includes a plurality of nodes, wherein at least a subset of the plurality of nodes are connected to indicate data flow among the at least a subset of the plurality of nodes, wherein the plurality of nodes includes a structure node, wherein the structure node represents control flow of data among one or more of the plurality of nodes;

generating a hardware description based on the graphical program, wherein the hardware description describes a hardware implementation of the graphical program, wherein said generating includes generating the hardware description based on the structure node;

configuring a programmable hardware element utilizing the hardware description to produce a configured hardware element, wherein the configured hardware element implements a hardware implementation of the graphical program.

2. The method of claim 1,

wherein the structure node indicates one of iteration, looping or conditional branching for the one or more of the plurality of nodes in the graphical program.

3. The method of claim 1,

wherein the structure node indicates a first portion of the graphical program, wherein the structure node indicates one of iteration, looping or conditional branching for the first portion of the graphical program.

4. The method of claim 1,

wherein the structure node contains a first portion of the graphical program, wherein the structure node indicates one of iteration, looping or conditional branching for the first portion of the graphical program.

5. The method of claim 4,

wherein the structure node includes an interior portion, wherein nodes comprised in the interior portion of the structure node execute according to control flow as indicated by the structure node;

wherein the first portion of the graphical program is comprised in the structure node.

6. The method of claim 1, wherein said generating includes examining one or more structure node parameters associated with the structure node, wherein said generating uses the one or more structure node parameters in generating the hardware description.

7. The method of claim 6, wherein the structure node is one of an iteration node or a looping node;

wherein the structure node includes at least one of a period parameter and a phase delay parameter, wherein the period parameter indicates a period of execution for cycles of the structure node, and wherein the phase delay parameter indicates a phase delay of cycles of the structure node.

8. The method of claim 1, wherein the structure node is an iteration node, wherein the iteration node indicates iteration of the one or more of the plurality of nodes in the graphical program for a plurality of times;

wherein the iteration node includes an iteration number which indicates a number of iterations for the first portion of the graphical program

wherein said generating uses the iteration number in generating the hardware description.

9. The method of claim 1, wherein the structure node is a looping node, wherein the looping node indicates looping of the one or more of the plurality of nodes in the graphical program for a plurality of times;

wherein the looping node includes a loop condition which indicates a number of executions for the first portion of the graphical program

wherein said generating uses the loop condition in generating the hardware description.

10. The method of claim 1, wherein said generating the hardware description based on the graphical program comprises converting each of said nodes into a hardware description format;

wherein, for said structure node, said converting comprises:

determining inputs and outputs to/from the structure node;

creating a hardware description of a control block which performs the control function indicated by the structure node;

traversing input dependencies of the node;

creating a hardware description of an AND gate, including listing connections of said input dependencies of the node to said AND gate.

11. The method of claim 1, wherein said generating the hardware description based on the graphical program comprises converting each of said nodes into a hardware description format;

wherein, for said structure node, said converting comprises:

determining inputs and outputs to/from the structure node;

accessing a hardware description of a control block which performs the control function indicated by the structure node from a library of hardware descriptions;

traversing input dependencies of the node;

creating a hardware description of an AND gate, including listing connections of said input dependencies of the node to said AND gate.

12. The method of claim 1,

wherein the graphical program implements a measurement function;

wherein the programmable hardware element is comprised in a device;

the method further comprising:

the device acquiring a signal from an external source after said configuring; and

the configured hardware element in the device executing to perform the measurement function on the signal.

13. The method of claim 12,

wherein the graphical program includes a block diagram and one or more panels, wherein the one or more panels operate as a user interface for the graphical program;

the method further comprising:

storing executable code corresponding to the one or more panels in a memory, wherein the executable code is executable to display the one or more panels on a display;

executing the executable code from the memory to present the one or more panels on the display during the configured hardware element in the device executing to perform the measurement function on the signal.

14. The method of claim 13,

wherein the one or more panels are useable for viewing the signal.

15. The method of claim 13,

wherein the one or more panels are useable for viewing input to and output from the programmable hardware element.

16. The method of claim 13,

wherein the one or more panels are useable for manipulating input to and viewing output from the programmable hardware element.

17. A system which generates a hardware implementation of graphical code, the system comprising:

a computer system comprising a processor and memory, wherein the memory stores a graphical program, wherein the graphical program includes a plurality of nodes, wherein at least a subset of the plurality of nodes are connected to indicate data flow among the at least a subset of the plurality of nodes, wherein the plurality of nodes includes a structure node, wherein the structure node represents control flow of data among one or more of the plurality of nodes; wherein the memory also stores a software program which is executable to generate a hardware description based on at least a portion of the graphical program, wherein the hardware description describes a hardware implementation of the at least a portion of the graphical program, wherein the hardware description includes a hardware description of the structure node;

a device coupled to the computer system, wherein the device includes a programmable hardware element;

wherein the computer system is operable to configure the programmable hardware element utilizing the hardware description to produce a configured hardware element, wherein the configured hardware element implements a hardware implementation of the at least a portion of the graphical program.

18. The system of claim 17,

wherein the structure node indicates one of iteration, looping or conditional branching for the one or more of the plurality of nodes in the graphical program.

19. The system of claim 17,

wherein the structure node indicates a first portion of the graphical program, wherein the structure node indicates one of iteration, looping or conditional branching for the first portion of the graphical program.

20. The system of claim 17,

wherein the structure node contains a first portion of the graphical program, wherein the structure node indicates one of iteration, looping or conditional branching for the first portion of the graphical program.

21. The system of claim 20,

wherein the structure node includes an interior portion, wherein nodes comprised in the interior portion of the structure node execute according to control flow as indicated by the structure node;

wherein the first portion of the graphical program is comprised in the structure node.

22. The system of claim 17, wherein the software program is operable to examine one or more structure node parameters associated with the structure node, wherein the software program uses the one or more structure node parameters in generating the hardware description.

23. The method of claim 22, wherein the structure node is one of an iteration node or a looping node;

wherein the structure node includes at least one of a period parameter and a phase delay parameter, wherein the period parameter indicates a period of execution for cycles of the structure node, and wherein the phase delay parameter indicates a phase delay of cycles of the structure node.

24. The system of claim 17, wherein the structure node is an iteration node, wherein the iteration node indicates iteration of the first portion of the graphical program for a plurality of times;

wherein the iteration node includes an iteration number which indicates a number of iterations for the first portion of the graphical program;

wherein the software program uses the iteration number in generating the hardware description.

25. The system of claim 17, wherein the structure node is a looping node, wherein the looping node indicates looping of the first portion of the graphical program for a plurality of times;

wherein the looping node includes a loop condition which indicates a number of executions for the first portion of the graphical program;

wherein the software program uses the loop condition in generating the hardware description.

26. The system of claim 17,

wherein the graphical program implements a measurement function;

wherein the device is operable to acquire a signal from an external source after being configured; and

wherein the configured hardware element in the device is operable to execute to perform the measurement function on the signal.

27. The system of claim 26,

wherein the computer system further includes a display;

wherein the graphical program includes a block diagram and one or more panels, wherein the one or more panels operate as a user interface for the graphical program;

wherein the memory of the computer system stores executable code corresponding to the one or more panels;

wherein the processor is operable to execute the executable code from the memory to present the one or more panels on the display during the configured hardware element in the device executing to perform the measurement function on the signal.

28. The system of claim 27,

wherein the one or more panels are useable for viewing the signal.

29. The system of claim 27,

wherein the one or more panels are useable for viewing input to and output from the programmable hardware element.

30. The system of claim 27,

wherein the one or more panels are useable for manipulating input to and viewing output from the programmable hardware element.

31. A. memory medium comprising program instructions for generating a hardware implementation of graphical code, wherein the program instructions are executable to implement:

creating a graphical program, wherein the graphical program includes a plurality of nodes, wherein at least a subset of the plurality of nodes are connected to indicate data flow among the at least a subset of the plurality of nodes, wherein the plurality of nodes includes a structure node, wherein the structure node represents control flow of data among one or more of the plurality of nodes;

generating a hardware description based on the graphical program, wherein the hardware description describes a hardware implementation of the graphical program, wherein said generating includes generating a hardware description based on the structure node;

configuring a programmable hardware element utilizing the hardware description to produce a configured hardware element, wherein the configured hardware element implements a hardware implementation of the graphical program.

32. The memory medium of claim 31,

wherein the structure node indicates one of iteration, looping or conditional branching for the one or more of the plurality of nodes in the graphical program.

33. The memory medium of claim 31,

wherein the structure node indicates a first portion of the graphical program, wherein the structure node indicates one of iteration, looping or conditional branching for the first portion of the graphical program.

34. The memory medium of claim 31,

wherein the structure node contains a first portion of the graphical program, wherein the structure node indicates one of iteration, looping or conditional branching for the first portion of the graphical program.

35. The memory medium of claim 34,

wherein the structure node includes an interior portion, wherein nodes comprised in the interior portion of the structure node execute according to control flow as indicated by the structure node;

wherein the first portion of the graphical program is comprised in the structure node.

36. The memory medium of claim 31, wherein said generating includes examining one or more structure node parameters associated with the structure node, wherein said generating uses the one or more structure node parameters in generating the hardware description.

37. The memory medium of claim 36, wherein the structure node is one of an iteration node or a looping node;

wherein the structure node includes at least one of a period parameter and a phase delay parameter, wherein the period parameter indicates a period of execution for cycles of the structure node, and wherein the phase delay parameter indicates a phase delay of cycles of the structure node.

38. The memory medium of claim 31, wherein the structure node is an iteration node, wherein the iteration node indicates iteration of the one or more of the plurality of nodes in the graphical program for a plurality of times;

wherein the iteration node includes an iteration number which indicates a number of iterations for the first portion of the graphical program

wherein said generating uses the iteration number in generating the hardware description.

39. The memory medium of claim 31, wherein the structure node is a looping node, wherein the looping node indicates looping of the one or more of the plurality of nodes in the graphical program for a plurality of times;

wherein the looping node includes a loop condition which indicates a number of executions for the first portion of the graphical program

wherein said generating uses the loop condition in generating the hardware description.

40. The memory medium of claim 31, wherein said generating the hardware description based on the graphical program comprises converting each of said nodes into a hardware description format;

wherein, for said structure node, said converting comprises:

determining inputs and outputs to/from the structure node;

creating a hardware description of a control block which performs the control function indicated by the structure node;

traversing input dependencies of the node;

creating a hardware description of an AND gate, including listing connections of said input dependencies of the node to said AND gate.

41. The memory medium of claim 31, wherein said generating the hardware description based on the graphical program comprises converting each of said nodes into a hardware description format;

wherein, for said structure node, said converting comprises:

determining inputs and outputs to/from the structure node;

accessing a hardware description of a control block which performs the control function indicated by the structure node from a library of hardware descriptions;

traversing input dependencies of the node;

creating a hardware description of an AND gate, including listing connections of said input dependencies of the node to said AND gate.

42. The memory medium of claim 31,

wherein the programmable hardware element is comprised in a device;

wherein the graphical program implements a measurement function for measuring a signal acquired by the device from an external source;

wherein the configured hardware element in the device is executable to perform the measurement function on the signal.

43. The memory medium of claim 42,

wherein the graphical program includes a block diagram and one or more panels, wherein the one or more panels operate as a user interface for the graphical program;

wherein the program instructions are further executable to implement:

storing executable code corresponding to the one or more panels in a memory, wherein the executable code is executable to display the one or more panels on a display; and

executing the executable code from the memory to present the one or more panels on the display during the configured hardware element in the device executing to perform the measurement function on the signal.

44. The memory medium of claim 43,

wherein the one or more panels are useable for viewing the signal.

45. The memory medium of claim 43,

wherein the one or more panels are useable for viewing input to and output from the programmable hardware element.

46. The memory medium of claim 43,

wherein the one or more panels are useable for manipulating input to and viewing output from the programmable hardware element.

47. A. memory medium comprising program instructions for generating a hardware implementation of graphical code, wherein the memory medium stores:

a graphical program, wherein the graphical program includes a plurality of nodes, wherein at least a subset of the plurality of nodes are connected to indicate data flow among the at least a subset of the plurality of nodes, wherein the plurality of nodes includes a structure node, wherein the structure node represents control flow of data among one or more of the plurality of nodes;

a software program for generating a hardware description based on the graphical program, wherein the hardware description describes a hardware implementation of the graphical program, wherein the software program generates the hardware description based on the structure node;

wherein the software program is executable to configure a programmable hardware element utilizing the hardware description to produce a configured hardware element, wherein the configured hardware element implements a hardware implementation of the graphical program.